



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ITW

Applicant: Scott R. Sahaida et al.

Title: SEMICONDUCTING DEVICE WITH STACKED DICE

Docket No.: 884.C31US1

Serial No.: 10/815,966

Filed: March 31, 2004

Due Date: March 8, 2006

Examiner: Deloris S. Bryant

Group Art Unit: 2813

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

- X Return postcard.
- X Response to Restriction Requirement (2 pgs.).

If not provided for in a separate paper filed herewith, Please consider this a **PETITION FOR EXTENSION OF TIME** for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Customer Number 21186

By: *Ann M. McCrackin*
Atty: Ann M. McCrackin
Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 1st day of March, 2006.

Chris Hammond
Name

Chris Hammond
Signature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)

S/N 10/815,966

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Scott R. Sahaida et al.

Examiner: Deloris Bryant

Serial No.: 10/815,966

Group Art Unit: 2813

Filed: March 31, 2004

Docket: 884.C31US1

Title: SEMICONDUCTING DEVICE WITH STACKED DICE

Assignee: Intel Corporation

Customer Number: 21186

RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the Restriction Requirement mailed February 8, 2006, Applicants hereby elect, with traverse, Group I (claims 1-11 and 22-26). **If the restriction is continued,** Applicants will cancel remaining claims 12-21 (with prejudice), and will reserve the right to reintroduce them in one or more divisional applications at a later date.

The Restriction Requirement is traversed on the basis that Restriction Requirements are optional in all cases. MPEP 803. If the search and examination of an entire application can be made without serious burden, the Examiner must examine it on the merits, even though it arguably may include claims to distinct or independent inventions. MPEP 803.

All of the pending claims relate to semiconducting devices, electronic systems and methods that include (i) a substrate; (ii) a first die attached to the substrate; (iii) a spacer covering the active circuitry on the upper surface of the first die where the spacer extends from a first side of the first die to an opposing second side of the first die and the spacer extends near a third side of the first die and an opposing fourth side of the first die such that the active circuitry is exposed near the third and fourth sides of the first die; and (iv) a second die stacked onto the spacer and the first die. The Examiner will be looking for a substrate, first and second dies and a spacer as recited in each of claims 1-26. Thus, Applicant respectfully submits that these claims can all be easily searched and examined together.

As part of maintaining the restriction, the Examiner states at page 2 of the Office Action that "the semiconductor device can be made without the active circuitry attached to the first die and the stacked die can be secured to each other without the use of a spacer but instead may be secured using an adhesive or conductive epoxy." Applicant can not see where the statement adequately indicates that claims 1-11 and 22-26 are distinct inventions from claims 12-21. Clarification is respectfully requested.

RESPONSE TO RESTRICTION REQUIREMENT

Serial Number: 10/815,966

Filing Date: March 31, 2004

Title: SEMICONDUCTING DEVICE WITH STACKED DICE

Assignee: Intel Corporation

Page 2

Dkt: 884.C31US1

In addition, Applicant also fails to see the relevance and accuracy of the statements because each of claims 1-26 recites a substrate, first and second dies and a spacer. Applicant further notes that the Examiner will be searching for each of these items (i) without regard to how the substrate, first and second dies and spacer are stacked; and (ii) with the first die including active circuitry on an upper surface of the first die.

The Examiner is invited to telephone Applicants' attorney Andrew Peret at 262-646-7009, or the below-signed attorney at 612-349-9592, to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SCOTT R. SAHAIDA ET AL.

By their Representatives,
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 349-9592

Date March 1, 2006 By Ann M. McCrackin
Ann M McCrackin
Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 1st day of March, 2006.

Chris Hammond
Name

Chris Hammond
Signature